AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A delay line unit of a delay locked loop (DLL) circuit, comprising:

a first delay line having a plurality of first unit delays, each first unit delay having a first delay, for delaying a clock signal;

a second delay line having a plurality of second unit delays, each second unit delay having a second delay, for delaying ~~the clock signal~~ an output of the first delay line if a delay locking operation is not achieved in the first delay line; and

a third delay line having a plurality of third unit delays, each third unit delay having a third delay, for delaying ~~the clock signal~~ an output of the second delay line if the delay locking operation is not achieved in the second delay line,

wherein the first delay is shorter than the second delay, and the second delay is shorter than the third delay.

2. (Original) The delay line unit as recited in claim 1, wherein the first, second and third delays are connected in series.

3. (Currently Amended) A delay locked loop (DLL) circuit used in a synchronous memory device, comprising:

a phase comparing unit for comparing a reference signal with a feedback signal and generating a comparison signal;

a delay controlling unit for generating a control signal in response to the comparison signal;

a delay line unit for delaying an internal clock signal in response to the control signal; and

a delay model for generating a feed back signal by delaying a clock signal,

wherein the delay line unit includes:

a first delay line containing a plurality of first unit delays, each first unit delay having a first resolution, for delaying the internal clock signal;

a second delay line containing a plurality of second unit delays, each second unit delay having a second resolution, for delaying ~~the clock signal~~ an output of the first delay line if a delay locking operation is not achieved in the first delay line; and

a third delay line containing a plurality of third unit delays, each third unit delay having a third resolution, for delaying ~~the clock signal~~ an output of the second delay line if the delay locking operation is not achieved in the second delay line~~.~~,

wherein the first resolution is lower than the second resolution, and the second resolution is lower than the third resolution.

4. (Previously Presented) The DLL circuit as recited in claim 3, wherein the first, second and third delay lines are connected in series.

5. (Cancelled)

6. (Currently Amended) A clock signal delay locking method in a delay locked loop (DLL) of a synchronous memory device, comprising the steps of:

a) generating a comparison signal for comparing a reference signal with a feedback signal generated from a delay model;

b) generating a control signal in response to the comparison signal; and

c) delaying a clock signal by using a delay line unit containing a plurality of unit delays, each unit delay having a different resolution each other, in response to the control signal,

wherein the step c) includes the steps of:

c1) delaying the clock signal through a first delay line containing a plurality of first unit delays, each having a first resolution;

c2) if a delay locking operation is not achieved in the step c1), delaying ~~the clock signal through~~ an output of the first delay line by a second delay line containing a plurality of second unit delays, each having a second resolution, which is higher than the first resolution; and

c3) if the delay locking operation is not achieved in the step c2), delaying ~~the clock signal through~~ an output of the second delay line by a third delay line containing a plurality of third unit delays, each having a third resolution, which is higher than the second resolution.

7. (Canceled)

8. (Previously Presented) The clock signal delay locking method as recited in claim ~~7~~ 6, wherein the first, second and third delay lines are connected in series.